



1AP7 Rec'd PCT/PTO 06 APR 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/552,877 ✓  
Applicant (s) : Kenneth E. Foster et al.  
Filed : October 12, 2005  
TC/A.U. : Unknown  
Examiner : Unknown  
Title : METHOD OF FILLING HIGH ASPECT RATIO, SMALL  
DIMENSION GAPS AND FORMULATIONS USEFUL  
THEREIN  
Docket No. : 62740A  
Customer No. 00109

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**INFORMATION DISCLOSURE STATEMENT**

Pursuant to Applicant's duty of disclosure under 37 CFR §1.56, the Examiner's attention is directed to the information identified in the attached Form PTO/SB/08a.

The cited U.S. patents and patent application publications are listed on Form PTO/SB/08a. A copy of the cited foreign patent documents and non-patent literature are enclosed herewith. The Examiner is requested to review each reference and formulate his/her own understanding thereof.

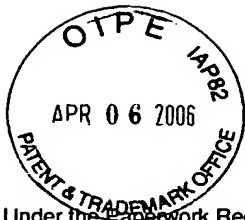
This Statement is being submitted before the mailing date of the first Office Action on the merits. Under 37 C.F.R. §1.97(b)(3), submission of this Statement requires no fee. If this is incorrect, please charge any fees required to Deposit Account No. 04-1512.

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Midland, MI 48641-1967  
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Respectfully submitted,

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PTO/SB/08A (08-03)

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Complete if Known**

Application Number	10/552877
Filing Date	April 15, 2004
First Named Inventor	Kenneth E. Foster
Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	62740A

Sheet 1 of 2

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US-5,965,679	Oct. 12, 1999	Godschalx et al.	
		US-6,280,794	Aug. 28, 2001	Tu et al.	
		US-6,352,591	March 5, 2002	Yieh et al.	
		US-6,458,647	Oct. 1, 2002	Tews et al.	
		US-2002/110665	Aug. 15, 2002	Edward et al.	
		US-2002/183476	Dec. 5, 2002	Kelly et al.	
		US-2002/198353	Dec. 26, 2002	Kreistler et al.	
		US-2004/0053033	Mar. 18, 2004	Niu et al.	
		US-6,646,081	Nov. 11, 2003	Godschalx et al.	
		US-5,446,204	Aug. 29, 1995	Bryant et al.	
		US-2004/0198850	Oct. 7, 2004	Connor et al.	
		US-6,559,215	May 6, 2003	Mills et al.	
		US-2004/0241338	Dec. 2, 2004	Foster et al.	
		US-			
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SignatureDate  
Considered

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STATEMENT BY APPLICANT**

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Sheet 2 of 2

Application Number	10/552877
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First Named Inventor	Kenneth E. Foster
Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	62740A

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
		Mouloud Bakli et al., "Materials and Processing for 0.25 micron Multilevel Interconnect," Microelectronic Engineering 33, (1997) 175-188.	<input checked="" type="checkbox"/>
		W.C. Gau et al., "Copper Electroplating for future ultralarge scale integration interconnection," J. Vac. Sci. Technology. A 18(2), 2000.	<input checked="" type="checkbox"/>
		John Baliga, "Options for CVD of Dielectrics Include Low-K Materials," Semiconductor International, Vol. 21, No. 6, 1998.	<input checked="" type="checkbox"/>
		Juseon Goo et al., "A highly Manufacturable, Low-Thermal Budget, Void and Seam Free Pre-Metal Dielectric Process Using new SOG for beyond 60nm DRAM and other devices," International Electronic Device Manufactures (IEDM), Session 12 paper 03, 2001.	<input checked="" type="checkbox"/>
		Jin-Hwa Heo et al., "Void Free and Low Stress Shallow Trench Isolation Technology using P-SOG for sub 0.1 micron Device," Symposium on VLSI section 14.1, 2002.	<input checked="" type="checkbox"/>
		S. J. Martin, et. al., Adv. Mater. 2000, 12, page 1769 & 1776, No. 23, December 1 (2000)	<input checked="" type="checkbox"/>
		Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing," 4th edition, McGraw-Hill, 2000, Chapter 1, page 14 and chapter 16, page 504-505.	<input checked="" type="checkbox"/>
		S.R. Wilson, et al., "Handbook of Multilevel Metalization for integrated circuits," Chapter 1 page 9, Noyes Publications, 1993.	<input checked="" type="checkbox"/>
		J.A. Mandelman, et al., "Challenges and Future Directions for the Scaling of Dynamic Random-access memory, IBM J. Res. & Dev., Vol. 46, No. 2/3 March/May 2002.	<input checked="" type="checkbox"/>
		Norio Sato et al., Jpn. J. Appl. Phys., Vol. 41, 2002. pp, 2367-2373.	<input checked="" type="checkbox"/>
		Seiichi Shishiguchi et al., " Process and design of production-ready equipment for Cu line-pillar/low-k STP interconnect technology." ASET.	<input checked="" type="checkbox"/>
		S. Shishiguchi, et al., "A CMP-Free Cu/Low-k Integration Technology by Cu Pillar/Line and ps-Low-k STP Process", ASET.	<input checked="" type="checkbox"/>
			<input type="checkbox"/>
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			<input type="checkbox"/>

Examiner Signature	Date Considered
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (option). <sup>2</sup>Applicant is to place a check mark here in English language Translation is attached.

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